REMARKS

This application has been reviewed in light of the Office Action dated March 17, 2005.

Claims 17-20 are presented for examination. Claim 17 has been amended to more particularly point out and distinctly claim the subject matter regarded as the invention. Claim 17 is the only independent claim. Favorable review is respectfully requested.

Claims 17-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Lauder et al. (U.S. Pat. No. 6,130,823) in view of Ahn et al. (U.S. Pat. 6,586,835). The applicants respectfully submit that amended independent claim 17 is patentable over the art cited by the Examiner, for the following reasons.

The present invention, as defined in claim 17, is directed to a semiconductor device having a plurality of chips. A support is attached to the chips on the back surfaces thereof; the chips are arranged on the support in a planar horizontal structure with a previously formed filling between the chips (see specification, Fig. 3D). Two additional layers are recited: (1) a first layer disposed on the front surfaces of the chips with a first surface being in contact with the front surfaces of the chips; and (2) a second layer attached to the first layer on the second surface of the first layer. It is explicitly recited that the chips separate the first layer from the support (see specification, e.g. Fig. 6A, where support 32 is separated from layer 26 by the chips). The second layer is recited as being formed of a solid dielectric material and having conducting pads thereon (see specification, page 7, line 31, to page 8, line 2). Furthermore, it is particularly pointed out that the second layer is of a solid dielectric material and includes electrical wiring connecting to the chips through the studs and the conducting pads, and that at least a portion of the electrical wiring runs within the second layer from one conducting pad to another conducting pad for making electrical connection between the chips.

Lauder et al. is understood to disclose a ball grid array module in which electronic devices 14 are disposed on a support 10, and are covered by an encapsulating layer 18 (Figure 1). The Examiner suggests that layer 18 is equivalent to the first layer in the present invention. In the present invention, however, the support and first layer are separated by the chips. Indeed, in the present invention the first layer may be prepared and joined to the chips before the support is prepared (see specification, Figures 3A-3D). Furthermore, since the chips are

arranged in a planar horizontal structure with a previously formed filling between the chips, the first layer of the present invention is not an encapsulating layer as in Lauder et al.

Lauder et al. states (col. 3, lines 9-14) that the electronic devices may be interconnected in a conventional manner. In addition, the interconnect pads of Lauder et al. serve to make vertical connections through vias between modules or from a device to a conductive ball. The interconnect pads of Lauder et al. do not contribute to chip-to-chip connections where the chips are arranged in a horizontal planar structure, as in the present invention. By referring to conventional electrical connections, Lauder et al. evidently suggests that wiring would be provided directly between devices and then covered by the encapsulating layer. This is contrary to the present invention, where a second layer (attached to an opposing surface of the first layer, and thus not in direct contact with the chips) includes the wiring for chip interconnections.

The Examiner suggests that heat transfer layer 34 of Lauder et al. is equivalent to the second layer of the present invention. The applicants wish to point out that layer 34 of Lauder et al. does not include any wiring for connections between chips, and in particular does not include any wiring running within the layer for connecting one chip with another. The only electrical paths present in layer 34 are the vertical connections between the vias and conductive balls. This is not at all equivalent to the wiring layer of the present invention, wherein an electrical signal between chips travels within the second layer from one conducting pad to another conducting pad. According to Lauder et al., interconnections between chips arranged horizontally (e.g. devices 14 on support 10) are to be made by conventional means. It therefore is submitted that Lauder et al. does not disclose or suggest a second layer (wiring layer) as in the present invention.

Ahn is understood to disclose a circuit package in which thermoelectric cooling is provided. Ahn does not disclose or suggest a semiconductor device with the features of the present invention. In particular, Ahn does not suggest a wiring layer in contact with a first layer making stud/via connections to chips, as in the present invention. It therefore is submitted that Ahn does not remedy the above-noted defects of Lauder et al. as a reference against the present invention. One might be motivated to combine Lauder et al. with Ahn to

provide a package with cooling to a ball grid array module. Such a combination clearly would not have the features of the present invention.

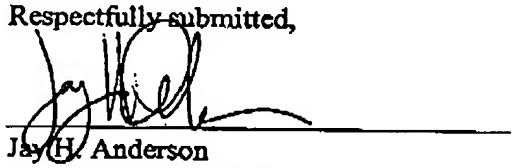
Accordingly, the invention of claim 17 would not have been obvious from either of the cited references, or from a combination thereof.

The other claims in this application are each dependent from the independent claim discussed above and are therefore believed patentable for the same reasons. Since each dependent claims are also deemed to define an additional aspect of the invention, however, the individual consideration of each on its own merits is respectfully requested.

In view of the foregoing amendments and remarks, the applicants respectfully request favorable consideration and early passage to issue of the present application.

The applicants' undersigned attorney may be reached by telephone at (845) 894-3667. All correspondence should continue to be directed to the below listed address.

Respectfully submitted,



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